BLF20M10LS200P

Power LDMOS transistor

AMPLEON

Rev. 1 — 8 January 2026 **Product data sheet**

1. Product profile

1.1 General description

200 W LDMOS-based power transistor suitable for use in industrial, scientific and medical applications and communication applications at frequencies from 1975 MHz to 2025 MHz.

The BLF20M10LS200P is designed for high-power CW applications and is assembled in a high performance ceramic package.

Table 1. Application information

RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C in a class-AB application circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW	2000	32	200	17.3	69.0
CW pulsed [1]	2000	32	200	17.6	67.2

[1] t_p = 100 µs; δ = 10 %.

1.2 Features and benefits

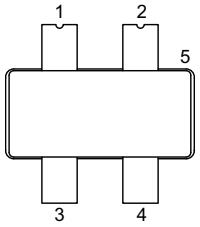
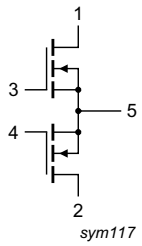
- High efficiency
- Excellent ruggedness
- Integrated ESD protection
- Internally input and output matched
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
  - Plasma generators
- Communications
  - Non cellular communications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT1121B	BLF20M10LS200PU	934961063112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−6	+9	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 45 °C; P_L = 200 W	0.34	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C, per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.0 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} =10 V; I_D = 104 mA	1.6	2.0	2.4	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 2.37 V; V_{DS} = 10 V	-	20.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 9 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 3.64 A	-	11.4	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 2.37 V; I_D = 3.64 A	-	118	-	mΩ

Table 7. RF characteristics

Test signal: pulsed RF; t_p = 100 µs; δ = 10 %; f = 2000 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 20 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 200 W	16.5	17.6	-	dB
RL_{in}	input return loss	P_L = 200 W	-	– 19	– 9	dB
η_D	drain efficiency	P_L = 200 W	62	67.8	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF20M10LS200P is capable of withstanding a load mismatch corresponding to VSWR ≥ 20 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 20 mA; P_L = 200W (CW); f = 2000 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 10 mA; V_{DS} = 32 V.

f	Z_S [1]	Z_L [1]
(MHz)	(Ω)	(Ω)
1975	3.84 – j4.92	2.89 – j3.48
2000	3.82 – j4.80	2.73 – j3.42
2025	3.80 – j4.68	2.58 – j3.35

[1] Z_S and Z_L defined in Figure 1.

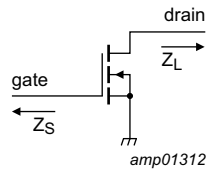
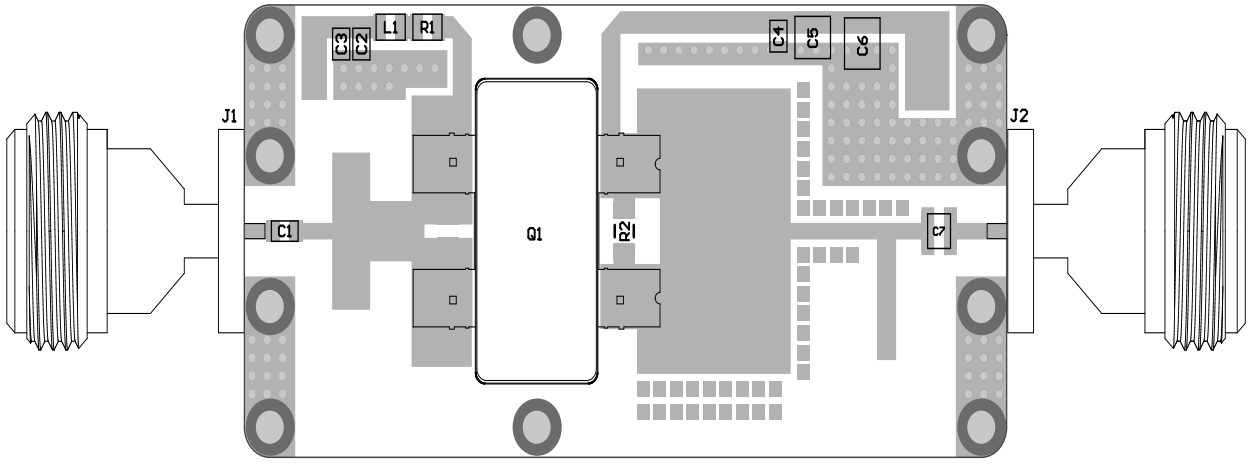


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): RF-35; ε_r = 3.5 F/m; thickness = 0.762 mm.

See Table 9 for a list of components.

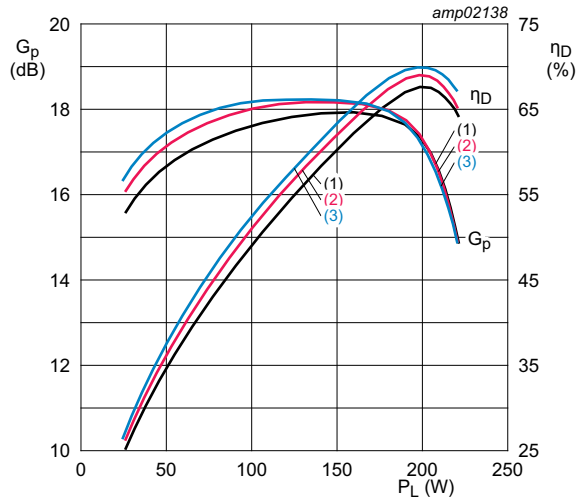
Fig 2. Component layout

Table 9. List of components

For test circuit see Figure 2.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	33 pF	ATC: ATC600F330JW250XT
C2, C4	multilayer ceramic chip capacitor	100 pF	ATC: ATC600F101JW250XT
C3	multilayer ceramic chip capacitor	4.7 μF	Murata: 0805 X7R
C5	multilayer ceramic chip capacitor	1000 pF	ATC: ATC800B102JW50XT
C6	multilayer ceramic chip capacitor	10 μF	TDK: C3225X7R2A106K
C7	multilayer ceramic chip capacitor	33 pF	ATC: ATC800R330BW500T
L1	square air core inductor	12 nH	Coilcraft: 0805HP-12NXGRC
R1	chip resistor	10 Ω	SMD 1206
R2	chip resistor	15 Ω	SMD 1206
Q1	LDMOS transistor		BLF20M10LS200P

7.4 Graphical data



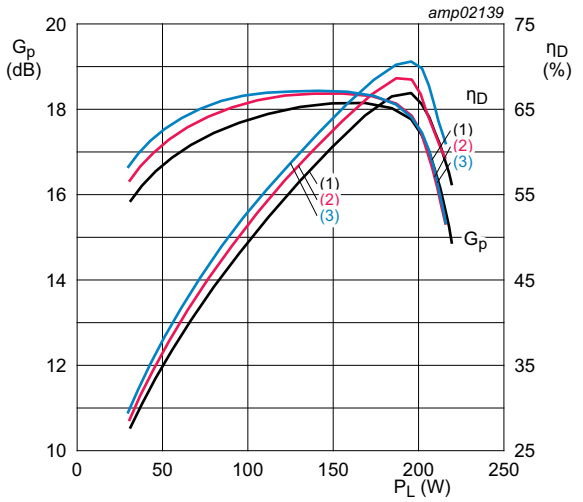
Test signal: CW: V_{DS} = 32 V; I_{Dq} = 20 mA.

(1) f = 1975 MHz

(2) f = 2000 MHz

(3) f = 2025 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



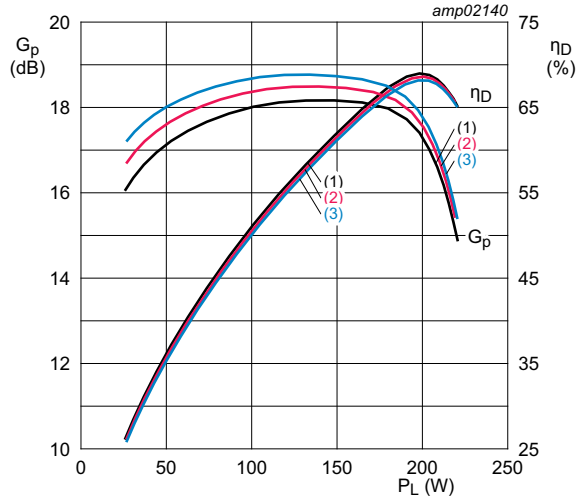
Test signal: CW pulsed: V_{DS} = 32 V; I_{Dq} = 20 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1975 MHz

(2) f = 2000 MHz

(3) f = 2025 MHz

Fig 4. Power gain and drain efficiency as function of output power; typical values



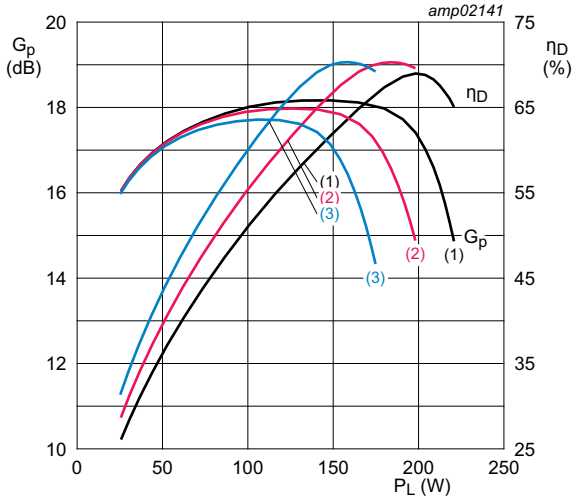
Test signal: CW; V_{DS} = 32 V; f = 2000 MHz.

(1) I_{Dq} = 20 mA

(2) I_{Dq} = 50 mA

(3) I_{Dq} = 100 mA

Fig 5. Power gain and drain efficiency as function of output power; typical values



Test signal: CW; I_{Dq} = 20 mA; f = 2000 MHz.

(1) V_{DS} = 32 V

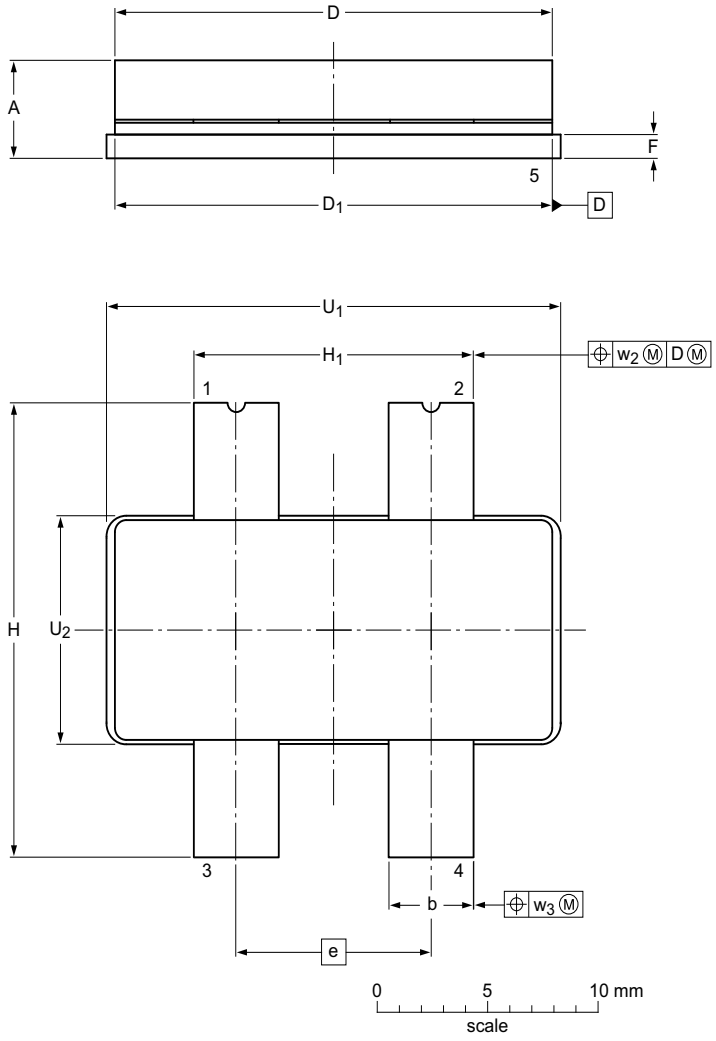
(2) V_{DS} = 30 V

(3) V_{DS} = 28 V

Fig 6. Power gain and drain efficiency as function of output power; typical values

8. Package outline

Earless flanged ceramic package; 4 leads **SOT1121B**



Dimensions

Unit[1]		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q	U_1	U_2	w_2	w_3	y
mm	max	4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	1.70	20.70	9.91	0.51	0.25	0.10
	nom						8.89											
	min	3.45	3.68	0.08	19.61	19.66		9.27	9.27	0.89	18.92	12.57	1.45	20.45	9.65			
inches	max	0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.067	0.815	0.39	0.02	0.01	0.004
	nom						0.35											
	min	0.136	0.145	0.003	0.772	0.774		0.365	0.365	0.035	0.745	0.495	0.057	0.805	0.38			

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1121B						~~12-06-07~~ 15-07-21

Fig 7. Package outline SOT1121B

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C3
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF20M10LS200P v.1	20260108	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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